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09/363,311	07/28/1999	DANIEL WATKINS	5201-16300/P	7985

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EXAMINER
BARAN, MARY C

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 04/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/363,311	Applicant(s) WATKINS, DANIEL	
	Examiner Mary Kate B Baran	Art Unit 2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Response to Amendment

1. This action is responsive to Amendments filed 04 March 2003. Claims 1-20 are pending. Claims 1, 11 and 17 have been amended.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 8, 9, 11-14 and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurosaka et al. (U.S. Patent No. 5,949,691), in view of McNamara et al. (U.S. Patent No. 6,141,630).

Referring to claim 1, Kurosaka et al. discloses a system for device verification (see Kurosaka et al., Figure 1, i.e. logic circuit verification device 100) comprising; a profile generation module (see Kurosaka et al., Figure 1, i.e. data input unit 101) configured to provide a pattern profile (see Kurosaka et al., Figure 1, i.e. intermediate format data file 106) that represents a test pattern, wherein the aspects are specified by a profile mode (see Kurosaka et al., column 8 lines 34-40), a coverage measurement module (see Kurosaka et al., Figure 1, i.e. corresponding point detection section 102) configured to process the pattern profile (see Kurosaka et al., Figure 1, i.e. intermediate format data file 106) to produce analysis results indicative of coverage provided by the

test pattern, wherein the profile generation module (see Kurosaka et al., Figure 1, i.e. data input unit 101) is further configured to process the analysis results to provide an improved pattern profile (see Kurosaka et al., column 9 lines 31-40), and a pattern generation module (see Kurosaka et al., Figure 1, i.e. corresponding point detection section 102) configured to receive the improved pattern profile and to convert the improved pattern profile into a test pattern for verifying device performance (see Kurosaka et al., column 8 lines 41-49). Kurosaka et al. does not teach a test pattern as a time sequence of input signal vectors with an associated sequence of output signal vectors.

McNamara et al. teaches a test pattern as a time sequence (see McNamara et al., column 4 lines 46-65) of input signal vectors (see McNamara et al., column 4 line 66 – column 5 line 4) with an associated sequence of output signal vectors (see McNamara et al., column 5 line 60 – column 6 line 7).

It would have been obvious to one having ordinary skill in the art to modify Kurosaka et al. to further include the teachings of McNamara et al. because using a test pattern with an associated output would have allowed the skilled artisan to verify if the system is working correctly and identify any system errors (see McNamara et al., column 6 lines 8-19).

Referring to claim 2, Kurosaka et al. further discloses a coverage measurement module which is configured to determine coverage of the test pattern by ascertaining if node faults are detectable, wherein node faults are detectable if running the test pattern

on a device would indicate a failure (see Kurosaka et al., column 11 lines 47-55 and column 11 line 60 – column 12 line 4).

Referring to claim 3, Kurosaka et al. further discloses a coverage measurement module which ascertains if node faults are detectable for those nodes in a first category and wherein the coverage of measurement module ignores those nodes in a second category. Where the nodes are categorized in the correspondence rules by logic type (see Kurosaka et al., column 8 lines 14-15) and the correspondence rules can then be used to select which nodes can be tested (see Kurosaka et al., column 7 lines 41-44).

Referring to claim 4, Kurosaka et al. further discloses a system further comprising a test pattern profiling module configured to convert an existing test pattern into a pattern profile as specified by a profile mode (see Kurosaka et al., column 7 lines 38-49).

Referring to claim 5, Kurosaka et al. further discloses a system further comprising a pattern checking module configured to process the pattern profile to produce analysis results indicative of whether the test pattern complies with a specified rule (see Kurosaka et al., column 10 lines 15-20).

Referring to claim 6, Kurosaka et al. teaches all features of the claimed invention except for a test generator which generates a set of test vectors that are then sent to a simulated design which models the operational characteristics of the circuit design.

McNamara et al. further discloses a test generator which generates a set of test vectors that are then sent to a simulated design which models the operational characteristics of the circuit design (see McNamara et al., column 3 lines 40-43 and column 3 lines 47-50).

It would have been obvious to one having ordinary skill in the art to modify Kurosaka et al. to further include the teachings of McNamara et al. because generating a set of test vectors which are sent to a simulated design to model the operational characteristics of the circuit design would have allowed the skilled artisan to thoroughly test the simulated device design.

Referring to claim 8, Kurosaka et al. teaches all the features of the claimed invention except for a simulated design which receives test vectors and generates output data.

McNamara et al. further teaches a simulated design which receives test vectors (i.e. input signals) and generates output data (see McNamara, column 3 lines 43-47).

It would have been obvious to one having ordinary skill in the art to modify Kurosaka et al. to further include the teachings of McNamara because using a simulated design to generate output data would have allowed the skilled artisan to test the specified modules more efficiently.

Referring to claim 9, Kurosaka et al. further discloses a data file which stores a detailed representation of the circuit information (see Kurosaka, column7 lines 6-9).

Referring to claim 11, Kurosaka et al. discloses a system for verifying device design that includes functional modules (see Kurosaka et al., Figure 1, i.e. logic circuit verification device 100), wherein the system comprises; a profile generation means (see Kurosaka et al., Figure 1, i.e. data input unit 101) for providing a pattern profile (see Kurosaka et al., Figure 1, i.e. intermediate format data file 106) that represents a test pattern, wherein the pattern profile includes an intelligible description of aspects of the test pattern, wherein the aspects are specified by a profile mode (see Kurosaka et al., column 8 lines 34-41), a coverage measurement means (see Kurosaka et al., Figure 1, i.e. corresponding point detection section 102) for analyzing the pattern profile to produce analysis results indicative of coverage provided by the test pattern, wherein the profile generation means is further configured to process the analysis results to provide an improved pattern profile (see Kurosaka et al., column 9 lines 31-40), and a pattern generation means for converting the improved pattern profile into a test pattern (see Kurosaka et al., column 8 lines 42-50). Kurosaka et al. does not teach a test pattern as a time sequence of input signal vectors with an associated sequence of output signal vectors.

McNamara et al. teaches a test pattern as a time sequence (see McNamara et al., column 4 lines 46-65) of input signal vectors (see McNamara et al., column 4 line 66

– column 5 line 4) with an associated sequence of output signal vectors (see McNamara et al., column 5 line 60 – column 6 line 7).

It would have been obvious to one having ordinary skill in the art to modify Kurosaka et al. to further include the teachings of McNamara et al. because using a test pattern with an associated output would have allowed the skilled artisan to verify if the system is working correctly and identify any system errors (see McNamara et al., column 6 lines 8-19).

Referring to claim 12, Kurosaka et al. further teaches a coverage measurement means which is configured to determine the coverage of the test pattern by ascertaining if node faults are detectable (see Kurosaka et al., column 11 line 60-64).

Referring to claim 13, Kurosaka et al. further discloses a test pattern profiling means for converting an existing test pattern into a pattern profile (see Kurosaka et al., column 7 lines 38-49).

Referring to claim 14, Kurosaka et al. teaches all the features of the claimed invention except that the pattern generation means is coupled to run the test pattern on a device simulation means that implements at least a portion of a device design.

McNamara et al. further discloses that the pattern generation means is coupled to run the test pattern on a device simulation means that implements at least a portion of a device design (see McNamara et al., column 5 line 60 – column 6 line 7).

It would have been obvious to one having ordinary skill in the art to modify Kurosaka et al. to further include the teachings of McNamara et al. because running the test pattern on a simulation which implements a portion of a device design would have allowed the skilled artisan to ensure a complete test of the design.

Referring to claim 16, Kurosaka et al. teaches that the device design includes functional modules each having module input signals and module output signals, and wherein the profile includes an intelligible representation of a test pattern for one of the functional modules.

McNamara et al. further teaches a simulated design which receives test vectors (i.e. input signals) and generates output data (see McNamara et al., column 3 lines 43-47), where a test generator generates test vectors based on a design description (see McNamara et al., column 4 lines 38-39) coded in a known design language (see McNamara et al., column 3 lines 22-24).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Kurosaka et al. to further include the teachings of McNamara et al. because including an intelligible representation of a test pattern would have allowed the skilled artisan to generate a more understandable process of the device design.

Referring to claim 17, Kurosaka et al. discloses a method for verifying a device design comprising the steps; analyzing a test pattern profile to determine coverage of a

test pattern (see Kurosaka et al., column 10 lines 62-63), generating a second profile for an improved test pattern that provides better coverage (see Kurosaka et al., column 10 lines 63-67), converting the second profile into the improved test pattern (see Kurosaka et al., column 10 line 67 – column 11 line 1) and running the improved test pattern on a simulated device (see Kurosaka et al., column 11 lines 2-3). Kurosaka et al. does not teach a test pattern as a time sequence of input signal vectors with an associated sequence of output signal vectors.

McNamara et al. teaches a test pattern as a time sequence (see McNamara et al., column 4 lines 46-65) of input signal vectors (see McNamara et al., column 4 line 66 – column 5 line 4) with an associated sequence of output signal vectors (see McNamara et al., column 5 line 60 – column 6 line 7).

It would have been obvious to one having ordinary skill in the art to modify Kurosaka et al. to further include the teachings of McNamara et al. because using a test pattern with an associated output would have allowed the skilled artisan to verify if the system is working correctly and identify any system errors (see McNamara et al., column 6 lines 8-19).

Referring to claim 18, Kurosaka et al. discloses a method where the test pattern profile includes an intelligible representation of aspects of the test pattern, and where the aspects are specified by the profile module (see Kurosaka et al., column 7 lines 38-41).

Referring to claim 19, Kurosaka et al. discloses a method where one aspect specified by the profile mode is a subset of input signals that represent instructions (see Kurosaka et al., column 7 lines 49-53).

Referring to claim 20, Kurosaka et al. teaches all the features of the claimed invention except that one aspect specified by the profile mode is a set of input signals for a functional sub-module of the device design.

McNamara et al. discloses a circuit design which is coded in a known software language and sent to a test generator which generates a set of test vectors that are then sent to a simulated design, which includes software, and this software then models the operational characteristics of the circuit design (see McNamara et al., column 3 lines 40-43 and column 3 lines 47-50).

It would have been obvious to one having ordinary skill in the art to modify Kurosaka et al. to further include the teachings of McNamara because breaking the input signals down by sub-modules of device design would have allowed the skilled artisan to ensure specific and relevant inputs to aid in detecting specific faults in the circuit design.

3. Claims 7, 10 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurosaka et al. (U.S. Patent No. 5,949,691), in view of McNamara et al. (U.S. Patent No. 6,141,630) and further in view of Valind (U.S. Patent No. 5,684,808).

Referring to claim 7, Kurosaka et al. and McNamara et al. teach all the features of the claimed invention except for a device design which has a set of interesting input signals and a set of customary input signals, wherein the profile includes a human-intelligible representation of the set of interesting input signals, and wherein the profile does not include any representation of the set of customary input signals.

Valind further discloses an automatic test pattern generator which is coupled to the detailed description (i.e. profile) and uses this information to generate test patterns for testing an integrated circuit (see Valind, column 8 lines 1-5), and a test generation function which automatically generates a test pattern to test for a determined fault (see Valind, column 11 lines 47-54).

It would have been obvious to one having ordinary skill in the art to modify Kurosaka et al. and McNamara et al. to further include the teachings of Valind because generating a test pattern to test for a determined fault would have allowed the skilled artisan to efficiently test all aspects of the circuit design.

Referring to claim 10, Kurosaka et al. and McNamara et al. disclose all the features of the claimed invention except for a profile generation module which is configurable to generate sequential permutations of values to specify pattern profiles.

Valind teaches test patterns which are generated using an automatic test pattern generator and then fault simulated to determine the faults detected by the given pattern (see Valind, column 10 lines 30-37).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kurosaka et al. to further include the teachings of Valind because generating sequential permutations of values to specify pattern profiles would have allowed the skilled artisan to ensure that all possible or relevant fault scenarios are covered.

Referring to claim 15, Kurosaka et al. and McNamara et al. teach all the features of the claimed invention except for a device design which has a first set of input signals and a second distinct set of input signals, wherein the profile includes an intelligible representation of the first set of input signals and wherein the profile does not include any representation of the second set of input signals.

Valind further discloses an automatic test pattern generator which is coupled to the detailed description (i.e. profile) and uses this information to generate test patterns for testing an integrated circuit (see Valind, column 8 lines 1-5), and a test generation function which automatically generates a test pattern to test for a determined fault (see Valind, column 11 lines 47-54).

It would have been obvious to one having ordinary skill in the art to modify Kurosaka et al. and McNamara et al. to further include the teachings of Valind because having a device design with two sets of input signals, one which is represented and one which is not would have allowed the skilled artisan to modify the device design input to match the design needs.

Response to Arguments

4. Applicant's arguments filed 04 March 2003 have been fully considered but they are not persuasive.

Applicant argues that none of the applied references teach "a pattern profile that represents a sequence of input signal vectors with an associated sequence of output signal vectors." However, while neither Kurosaka nor Valind are used to reject this limitation, it is considered met by McNamara et al. In McNamara et al., the design is tested with input values (i.e. input signal vectors) to determine stability (see McNamara et al., column 5 lines 10-14); thus the output is compared with expected results (i.e. output signal vectors) and it is determined if the output is correct or incorrect (see McNamara et al., column 5 lines 15-31, and column 5 line 60 – column 6 line 7). Test vectors are created by the test generator and "generate input signals" by setting variables (see McNamara et al., column 6 lines 40-44) so that all paths can be tested and an output can be generated and compared to the expected values (see McNamara et al., column 6 lines 1-7). Therefore the Examiner concludes that McNamara et al. does teach the claimed limitation.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary Kate B Baran whose telephone number is (703) 305-4474. The examiner can normally be reached on Monday - Friday from 8:00 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S Hoff can be reached on (703) 308-1677. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

MKB
April 14, 2003

MARC S. HOFF
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